REMARKS

Claims 1-11 are pending; and claims 8-11 are newly added in accordance with current Office policy, to alternatively define Applicant's invention and thereby assist the Examiner by facilitating the search and thus expediting the compacted prosecution.

Claims 1 and 2 were rejected under 35 U.S.C. §103(a), as rendered obvious and unpatentable, over Krause in view of Kitou et al. (*hereafter:* Kitou). The Applicant respectfully traverses this rejection for the following reason(s).

Krause discloses a technique to inject a DC current into a horizontal deflection yoke to achieve raster shifting to offset symmetry problems in the yoke and CRT gun system. The DC current (which is bi-directional) is used to unbalance the scan current, thereby providing a means to shift the horizontal scan raster to the left and right.

The applicant's invention is directed towards a display device with a power interruption delay function for gradually lowering an input voltage to a H/V processor constant voltage circuit when power supplied to the display device is interrupted. Krause makes no mention of such a power interruption delay function.

Kitou discloses a source-voltage controlling high voltage stabilizer for detecting the high voltage and controlling the source voltage, while providing a detector for detecting the envelope of a horizontal deflection current. Kitou makes no mention of a power interruption delay function.

Krause does have one delay feature disclosed, but Kitou does not. Krause discloses that there is an objective, satisfied by the circuit of FIG. 6, to generate a gate control signal for transistor switch M1, which will not be affected by the modulation of the transistor's drain/source voltage by the S-correction and Scan-supply voltage rail which can vary from 50 V to 150 V depending on the horizontal scan frequency. S-correction is required to symmetrically modulate the H-scan current through the deflection coils, to correct raster distortion introduced due to the radius of the CRT face. In operation, the above mentioned objective is accomplished as follows.

A 5 volt peak to peak control signal is applied via the resistor R4 to the base of the transistor T2. The collector current of the transistor T2 will generate across the resistor R1 the necessary voltage Vgs to switch the N-channel MOSFET M1 on and off. By choosing the value of the resistor R1 to be two times that of the resistor R2, a negative voltage Vgs of about 9 V will be generated. With this arrangement, the drain voltage can float freely without affecting the Vgs voltage. The timing of the control signal is designed to keep the transistor M1 off during retrace and to increase the DC current by advancing the leading negative edge of the voltage Vgs (701 in FIG. 7) towards the start of the trace period. The maximum current will be generated by having the transistor M1 on during a complete trace period. The DC current is decreased by **delaying** the edge 701 further from the start of the trace period. In this manner, the conduction time of the transistor M1 can be varied from zero to full on, and the available raster shift current can be varied from 0 to about 1A. Krause makes no further mention of a delay function.

Accordingly, the feature of *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said*

display device is interrupted set forth in claim 1 is deemed to be non-obvious in view of the proposed combination of Krause and Kitou.

It noted here that the Examiner has not identified where the foregoing feature of claim 1 is found in the applied art. Note, *Ex parte Levy*, 17 USPQ2d 1461, 1462 (1990) states:

> "it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference."

Additionally, since the proposed combination of Krause and Kitou fails to teach or suggest the feature of *power interruption delay charging means* as noted above, then it is clear that the features of *said power interruption delay charging means [including] a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted, and a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted* are non-obvious with regard to the applied art.

It is noted here that the Examiner refers to Krause, col. 6, lines 8-25, *i.e.,* claims 2-5 of Krause. A review of claims 2-5 of Krause finds no mention of *power interruption delay charging means*. Note that, in Krause, claim 2 is directed towards a switching means (M1 and M2) responsive to a raster shift control signal for applying a charging voltage to the horizontal deflection coil DY to cause a controlled DC current to flow in the deflection coil, the switching means comprising first means for applying the charging voltage to the horizontal deflection coil with a first polarity and second means for applying the charging voltage to the horizontal deflection coil with a second

polarity; claim 3 is directed towards a means, comprising a transformer T1 including a secondary coil, the secondary coil being connected to a storage capacitor C1, responsive to a retrace voltage for charging a storage capacitor to a charging voltage; claim 4 is directed towards the means for charging further comprising a diode (D1, D2) connected between the secondary coil and the storage capacitor C1; and claim 5 is directed towards the first means which comprises an electronic switch (M1, M2) connected between the storage capacitor C1 and the diode (D1, D2) and first control means connected to the electronic switch for turning said electronic switch on and off.

Krause fails to teach or suggest that capacitor C1 has the function of *performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted.* Krause also fails to teach or suggest that either of diodes D or D2 has the function of *preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.* The Examiner has not applied Kitou in this regard.

Accordingly, claims 1 and 2 are deemed to be non-obvious in view of the proposed combination of Krause and Kitou. Therefore, the rejection of claims 1 and 2 is deemed to be in error and should be withdrawn.

Claim 3 was rejected under 35 U.S.C. §103(a), as rendered obvious and unpatentable, over Yang in view of Krause. The Applicant respectfully traverses this rejection for the following reason(s).

Yang is directed towards a switching power supply for converting input alternating current (referred to hereinafter as AC) power to direct current (referred to hereinafter as DC) power and Krause discloses a technique to inject a DC current into a horizontal deflection yoke to achieve raster shifting to offset symmetry problems in the yoke and CRT gun system. The DC current (which is bi-directional) is used to unbalance the scan current, thereby providing a means to shift the horizontal scan raster to the left and right. The Examiner's reasons for combining Yang and Krause is untenable. The Examiner erroneously suggests that it would have been obvious to utilize Krause's horizontal deflection circuitry with Yang's switching power supply "because it would lower power losses." It is not clear how modifying Yang to include the horizontal deflection circuitry of Krause would lower power losses in Yang.

Additionally, claim 3 calls for

> *power interruption delay charging means for gradually lowering said DC input voltage received by said horizontal deflection circuit when said AC power supplied to said power supply circuit is interrupted, said power interruption delay charging means comprising:*
>
> *a polarity capacitor for performing a charging operation when said AC power is supplied and a discharging operation when said AC power is interrupted; and*
>
> *a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to said power supply circuit when said AC power is interrupted.*

The Examiner has not indicated how the art is being applied with regard to the *power interruption delay charging means*, however, the Examiner relies on Krause only in regard to a horizontal deflection circuit under the control of a microcomputer. With respect to Yang, the Examiner did make mention of a "polarity capacitor connected to the diode" and referred to col. 8,

lines 7-63. Note here that col. 8, lines 7-63 are directed towards claims 10-14 of Yang. It is not understood why the Examiner could not be more particular with regard to the which capacitor and which diode are being relied on in the rejection, since Yang clearly provides numerous figures with several diodes and capacitors and these diodes and capacitors each have reference numerals. Now, looking to claims 10-14 of Yang, there is no mention of *power interruption delay charging means for gradually lowering said DC input voltage... when said AC power supplied to said power supply circuit is interrupted.* It is required by claim 3 that the *power interruption delay charging means* comprise *a polarity capacitor for performing a charging operation when said AC power is supplied and a discharging operation when said AC power is interrupted.* Again, looking to Yang's claims, we find no mention of such a polarity capacitor. Note that Yang describes capacitor 31 and 35 as "filtering capacitors" and never describes them as *performing a charging operation when said AC power is supplied and a discharging operation when said AC power is interrupted.* It is well known in the art that filtering capacitors 31 and 35 are utilized to smooth a ripple component of the DC voltages at the rectifying diodes 25 and 33 (see Fig. 4). Note also, that claims 10-14 in Yang fail to mention that any of diodes 25, 27 or 33 has a function of *preventing a voltage charged on said polarity capacitor from being discharged to said power supply circuit when said AC power is interrupted*, instead diodes 25 and 33 are rectifying diodes and diode 27 is a fly-wheel diode which functions to allow the current to continuously flow through the filtering choke coil 29.

Deficiencies in the factual basis cannot be supplied by resorting to speculation or unsupported generalities. *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967) and *In re Freed*, 425 F.2d 785, 165 USPQ 570 (CCPA 1970).

Accordingly, the rejection of claim 3 is deemed to be in error and should be withdrawn.

Claim 4 was rejected under 35 U.S.C. §103(a), as rendered obvious and unpatentable, over Yang in view of Krause as applied to claim 3 and in further view of Kitou. The Applicant respectfully traverses this rejection for the following reason(s).

Kitou fails to provide any teaching or suggestion of the *power interruption delay charging means* of claim 3. Kitou has been applied with respect to the *current amplifier for amplifying current in response to said pulse width modulation signal generated by said pulse width modulation controller* and the *H/V processor constant voltage circuit for supplying a constant voltage* to a H/V processor.

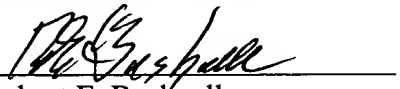
Therefore, since claim 4 depends from claim 3 and includes, by definition of a dependent claim, all the features of claim 3, the proposed combination of Yang, Krause and Kitou fails to teach all the features set forth in the pending claims. Accordingly, the rejection of claim 4 is deemed to be in error and should be withdrawn.

The indication of allowable subject matter with respect to claims 5-7 is appreciated. New claim 8 is a combination of claims 1 and 5 and is therefore deemed to be allowable over the art in view of the allowable subject matter of claim 5. Claims 9-11 depend from claim 8 and are deemed to be allowable for the same reasons.

The examiner is respectfully requested to reconsider the application, withdraw the objections and/or rejections and pass the application to issue in view of the above amendments and/or remarks.

No fee is incurred by this Amendment.

Respectfully submitted,



Robert E. Bushnell
Attorney for Applicant
Reg. No.: 27,774

1522 K Street, N.W.
Washington, D.C. 20005
(202) 638-5740

Folio: P54766
Date: 8/24/99
I.D.: REB/MDP